REMARKS

This paper is responsive to the Non-Final Office Action dated August 1, 2005. Claims 1-22 and 24-42 were examined. Claims 1-7, and 26-42 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,519,175 to Sadayuki. Claims 8-22 and 24-25 are allowed.

Claim Rejections - 35 U.S.C. § 102

Claims 1-7, and 26-42 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,519,175 to Sadayuki. Regarding claim 1, Applicants respectfully maintain that Sadayuki, alone or in combination with other references of record, fails to teach or suggest

> a test block for a memory circuit, wherein the test block is configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors,

as recited by claim 1. The Office Action relies on Figure 10 of Sadayuki to supply this teaching. This portion of Sadayuki teaches an offset control signal generating circuit (col. 15, lines 42-54). The offset control signal generating circuit of Sadayuki sets control signals RO1 to RO6 of Figure 11 to generate offset control signal OFS based on a desired offset level written from an I/O terminal into the offset setting memory cell array 80 (col. 15, lines 30-33). The offset control signal of Sadayuki is used to set the offset level of a sense amplifier by setting the gate potential of a MOS transistor for offset generation to generate a reference level for a ferroelectric memory device without the use of a dummy cell (Abstract). The circuit of Figure 10 of Sadayuki teaches setting the offset control signal based on a configuration stored in memory. The circuit of Figure 10 of Sadayuki does not characterize the sensing offset of the sensing circuit, as required by claim 1. Sadayuki merely teaches that the most suitable potential of the offset control signal OFS may be determined by performing a test of the reading operation of the ferroelectric memory device while applying various voltages from outside by use of a pad (col. 13, lines 52-64; col. 15, lines 62-66), but Sadayuki fails to teach or suggest how this detection is performed and further fails to teach or suggest characterization in situ of a sensing offset of a sensing

including a cross-coupled pair of transistors, as required by claim 1. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 2, Applicants respectfully maintain that Sadayuki, alone or in combination with other references of record, fails to teach or suggest that

> the test block selectively introduces discharge paths into respective halves of a differential circuit sensed by the sensing circuit,

as required by claim 2. The Office Action relies on col. 11, lines 40-63 of Sadayuki to supply this teaching. This portion of Sadayuki teaches a memory cell array 10A and a sense amplifier 20C coupled to data lines DL1 and DL2 (Figure 6; col. 11, lines 40-50). N-type MOS transistor of Figure 6 of Sadayuki introduces an offset to sense amplifier 20C (col. 11, lines 69-63). This circuit structure of Sadayuki teaches generating a reference level without the use of a dummy cell (col. 11, lines 59-63). Nowhere does Sadayuki teach or suggest that a test block selectively introduces discharge paths into respective halves of a differential circuit sensed by the sensing circuit, as required by claim 2. Accordingly, Applicants respectfully request that the rejection of claim 2 and all claims dependent thereon, be withdrawn.

Regarding claim 5, Applicants respectfully maintain that Sadayuki, alone or in combination with other references of record, fails to teach or suggest that

> a sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors,

as required by claim 5. The Office Action relies on Figures 7-8 and col. 12, lines 1-65 of Sadayuki to supply this teaching. These portions of Sadayuki teach that an offset intentionally introduced into the sense amplifier is based on the gate voltage and the threshold voltage of p-type MOS transistor 30 (col. 12, lines 8-18). The absolute value of the threshold voltage of the p-type MOS transistor 30 of Sadayuki is the median value between the bit lines signal voltage when the data '0' in the memory cell is read out and the bit line signal voltage when the data '1'

is read out. Nowhere does Sadayuki teach or suggest that a sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors, as required by claim 5. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Regarding claim 26, Applicants respectfully maintain that Sadayuki, alone or in combination with other references of record, fails to teach or suggest

> selectively configuring a pair of discharge paths in a first configuration and introducing the pair of discharge paths into respective halves of a differential circuit,

as required by claim 26. The Office Action apparently relies on col. 11, lines 40-63 of Sadayuki to supply this teaching. This portion of Sadayuki teaches a memory cell array 10A and a sense amplifier 20C coupled to data lines DL1 and DL2 (Figure 6; col. 11, lines 40-50). N-type MOS transistor of Figure 6 of Sadayuki introduces an offset to sense amplifier 20C (col. 11, lines 69-63). This circuit structure of Sadayuki teaches generating a reference level without the use of a dummy cell (col. 11, lines 59-63). Nowhere does Sadayuki teach or suggest that a test block selectively configuring a pair of discharge paths in a first configuration and introducing the pair of discharge paths into respective halves of a differential circuit, as required by claim 26. Accordingly, Applicants respectfully request that the rejection of claim 26 and all claims dependent thereon, be withdrawn.

Regarding claim 41, Applicants respectfully maintain that Sadayuki, alone or in combination with other references of record, fails to teach or suggest

> means for detecting in situ a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors,

as recited by claim 41. The Office Action relies on Figure 10 of Sadayuki to supply this teaching. This portion of Sadayuki teaches an offset control signal generating circuit (col. 15, lines 42-54). The offset control signal generating circuit of Sadayuki sets control signals RO1 to

RO6 of Figure 11 to generate offset control signal OFS based on a desired offset level written from an I/O terminal into the offset setting memory cell array 80 (col. 15, lines 30-33). The offset control signal of Sadayuki is used to set the offset level of a sense amplifier by setting the gate potential of a MOS transistor for offset generation to generate a reference level for a ferroelectric memory device without the use of a dummy cell (Abstract). The circuit of Figure 10 of Sadayuki teaches setting the offset control signal based on a configuration stored in memory. The circuit of Figure 10 of Sadayuki does not detect the sensing offset of the sensing circuit, as required by claim 41. Sadayuki merely teaches that the most suitable potential of the offset control signal OFS may be determined by performing a test of the reading operation of the ferroelectric memory device while applying various voltages from outside by use of a pad (col. 13, lines 52-64; col. 15, lines 62-66), but Sadayuki fails to teach or suggest how this detection is performed and further fails to teach or suggest detecting in situ of a sensing offset of a sensing including a cross-coupled pair of transistors, as required by claim 41. Accordingly, Applicants respectfully request that the rejection of claim 41 and all claims dependent thereon, be withdrawn.

Allowable Subject Matter

Applicants appreciate the allowance of claims 8-22 and 24-25.

Summary

Claims 1-22 and 24-42 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

PATENT

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